operation to write a write data by the second unit from an external device in the target page after performing the cell data initializing operation,

the error correction circuit:

reads a reset codeword by the second unit from the target page, the reset codeword including a reset main data and a reset parity data, the reset main data and the reset parity data including the initializing bits;

corrects at least one error in the reset main data using the reset parity data; and

generates a write parity data based on the write data and a portion of the reset main data, and

the I/O gating circuit writes the write data and the write parity data in the target page.

9. The semiconductor memory device of claim **8**, wherein the error correction circuit comprises:

an ECC encoder configured to read the reset codeword to correct the at least one error in the reset main data; and

an ECC decoder configured to generate the write parity data based on the write data and some of the reset main data.

10. The semiconductor memory device of claim **8**, wherein the target page includes a normal region that stores the main data and a parity region that stores the write parity data.

11. The semiconductor memory device of claim **1**, wherein each of the memory cells includes one of a dynamic memory cell and a resistive type memory cell.

12. The semiconductor memory device of claim **1**, wherein the I/O gating circuit is configured to perform the cell data initializing operation during a power-up sequence of the semiconductor memory device.

13. A memory system comprising:

at least one semiconductor memory device; and

a memory controller configured to control the at least one semiconductor memory device, wherein the at least one semiconductor memory device comprises:

a memory cell array including a plurality of memory cells;

an input/output (I/O) gating circuit configured to, before performing a normal memory operation on the memory cell array by a first unit, perform a cell data initializing operation by writing initializing bits in the memory cell array by a second unit different from the first unit; and

an error correction circuit configured to perform an error correction code (ECC) encoding and an ECC decoding on a target page of the memory cell array by the second unit, based on the initializing bits.

14. The memory system of claim **13**, wherein the first unit corresponds to a prefetching unit of the semiconductor memory device when the semiconductor memory device performs a read operation or a write operation, the second unit corresponds to a codeword unit of the semiconductor memory device, the codeword unit is greater than the prefetching unit, and the memory cell array is a three-dimensional memory cell array.

15. The memory system of claim **13**, wherein the at least one semiconductor memory device includes a plurality of semiconductor memory devices mounted on a module board,

the memory controller applies one of an initializing write command and a power-up signal to each of the semiconductor memory devices, and

each of the semiconductor memory devices performs the cell data initializing operation in response to one of the initializing write command and the power-up signal.

16. A semiconductor memory device comprising:

a memory cell array;

a control circuit configured to control a cell data initializing operation on the memory cell array by a unit of a codeword to initialize the memory cell array in a codeword state, prior to performing a normal access to the memory cell array by a unit of a prefetch, a size of the codeword unit being greater than a size of the prefetch unit.

17. The semiconductor memory device of claim **16**, wherein the control circuit performs the cell data initializing operation by writing initializing bits in the memory cell array by the unit of the codeword.

18. The semiconductor memory device of claim **17**, wherein the control circuit is further configured to perform an error correction code (ECC) encoding and an ECC decoding on a target page of the memory cell array by the prefetch unit, based on the initializing bits.

19. The semiconductor memory device of claim **18**, wherein the target page includes a normal region that stores main data and a parity region that stores write parity data.

20. The semiconductor memory device of claim **16**, wherein memory cells of the memory cell array comprise a magnetoresistive random access memory (MRAM).

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